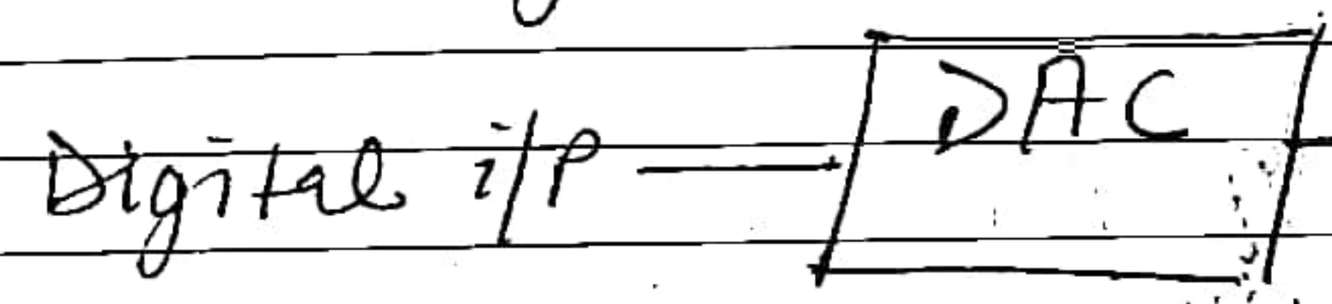
Unit - 4

Digital to Analog and Analog to digital converters.

DAC - Digital to Analog Convertors
(Decoding Device)

- Converts a digital i/p signal into an analog output signal
- The digital signal is represented with a binary code, which is combination of bits 0 and 1.

Block Diagram



- It consist of a number of binary inputs and a single output

Types of DAC

1. Weighted Resistor DAC
2. R-2R Ladder DAC

Weighted Resistor DAC - It produces a analog output, which is almost equal to the digital input by using binary weighted resistors.

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128-237 (WK - 19)

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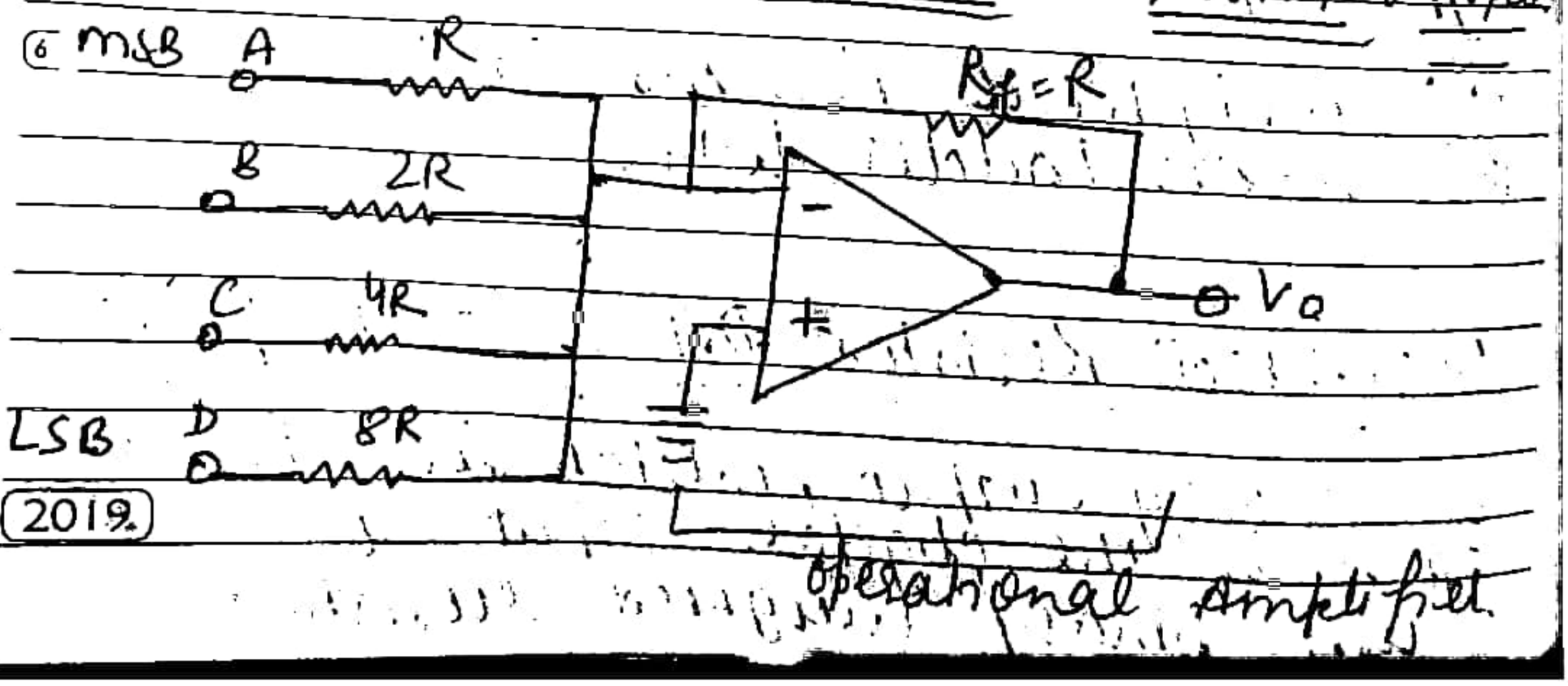
In the inverting adder circuit
- Binary weighted resistor DAC is called as weighted resistor DAC
- It is also called decoding device
- It is a simple method where each bit signal is connected with weighted resistor
- MSB is connected to lowest resistor LSB is it is highest value resistance
- As we move from MSB to LSB, the resistance value is made twice of previous resistor.
- The purpose of using the R value is to pass minimum current through LSB while maximum current through MSB.
- The n/w connected in this method is also known as "Variable Resistor N/w"



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- summing amplifier is used
- The i/p to the ckt can be connected by using four switches so that each switch can be either at 0 level or 1 level.

$$V_{out} = -R_f\left(\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c}\right)$$

When we take ABCD bits.

$R_f = R$ so

$$V_o = -R\left(\frac{A}{R} + \frac{B}{2R} + \frac{C}{4R} + \frac{D}{8R}\right)$$

$$V_o = -\left(\frac{A}{2^0} + \frac{B}{2^1} + \frac{C}{2^2} + \frac{D}{2^3}\right)$$

Let's take two voltage level 0=0, 1=4V.

① when i/p ABCD = 0000

$$V_o = -\left(\frac{0}{2^0} + \frac{0}{2^1} + \frac{0}{2^2} + \frac{0}{2^3}\right) = 0V$$

② when ABCD = 0001

$$V_o = -\left(\frac{0}{2^0} + \frac{0}{2^1} + \frac{0}{2^2} + \frac{4}{8}\right)$$

$$= -0.5V$$

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130-235 (WK · 19)

(5) when ABCD = 0010

$V_o = -\left(\frac{4}{4}\right) = -1V.$

(4) when ABCD 0011

$V_o = -\left(\frac{4}{4} + \frac{4}{8}\right) = -1.5V$

(5) when ABCD = 0100

$V_o = -2V$

and so on.

so there will be output that are directly proportional to digital i/p

Drabacks

(1) Each R has a different value. C is exactly half of the previous one, such precision resistors may not be available. It requires a wide range of resistors.

(2) Each R handles diff value of current so all have different voltages.

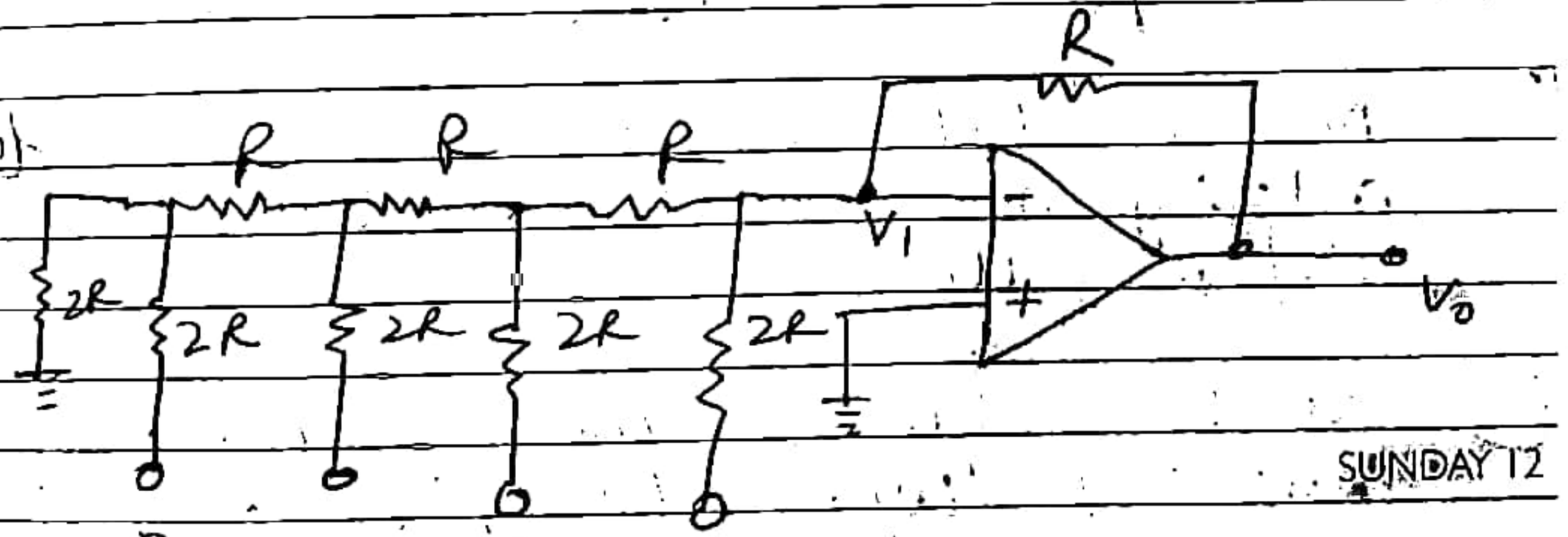
(3) The MSB R is required to handle a large current

(4) Any change in temperature will cause change in resistance, ∴ will effect the o/p voltage.

(5) To overcome these problems an alternative circuit of R-2R ladder has been developed

R-2R D/A Convertor

- Resistive n/w contains only two resistors value R and 2R
- It has OPAMP as a scaling ckt.
- MSB towards right and LSB i/p with left of the ckt.



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Vertical resistors are = 3×2R
horizontal " " = 4R

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$$V_0 = -\left(\frac{A}{2^1} + \frac{B}{2^2} + \frac{C}{2^3} + \frac{D}{2^4}\right)$$

When ABCD = 0000

$V_0 = 0$

(2) ABCD = 0001 ; $V_0 = -0.625$

(3) ABCD = 0010 ; $V_0 = -1.25$

(4) ABCD = 0011 ; $V_0 = -1.875$

Advantages =

(1) Easier to build accurately as only two precision R and required

(2) No of bits can be expanded by adding more sections of same R/2R values

(3) Node voltage remains same or constant with changing input binary words

(4) The process is comparatively fast

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parameter to be considered while selecting a DAC for a particular application

specifications of D/A converters.

① Resolution - The small change in the analog value when there is a change in the digital signal is called Resolution

- The value of resoultion is required to be very higher.

- The resolution is calculated by using the formula = 2^n

no no. of bits

if n = 4

Resoultion = $2^4 = 16$

if n = 3

Resoultion = $2^3 = 8$

Resout Resolution = $\frac{VFS}{2^N - 1}$

full scale value of voltage

② Accuracy Deviation of the Actual output voltage with the theoritical value

- It indicates how the actual o/p voltage is close to the

theoritical value
- it depends on the accuracy of the resistors used. and various parameters of OPAMP.
- Accuracy should be as high as possible.

Linearity - There should be a linear relationship b/w analog o/p voltage and digital i/p value.
Ideally it should provide the linear relationship but practically not possible.

Temperature Sensitive - o/p should not vary as according to the change in temperature it should possible the stable output.

Speed - It depends on how fast we get desired output after providing the input.
- Conversion time should be as small as possible.
- Conversion time means time required to change the digital signal into analog signal.

Settling time the analog o/p requires certain time to settle down to a single value.

Long letter draft -

supply rejection - if there is any change in the i/p voltages, then the other parameters or characteristics of A.D.C. should not vary.

Sample and Hold Circuit

- This is one of the application of OPAMP, OTAMP,
- Sample and hold circuits are basically used in the s/m where it's is imp. to sample of the value of i/p voltage and hold it for a certain period of time.
- Basic concept behind sample and hold circuit
- There are two process
  (1) sampling the i/p signal
  (2) hold the sampled value for a specific period of time

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137-228 (WK - 20)

→ continuous data converted into discrete signal
→ the DT signal is converted into finite signal

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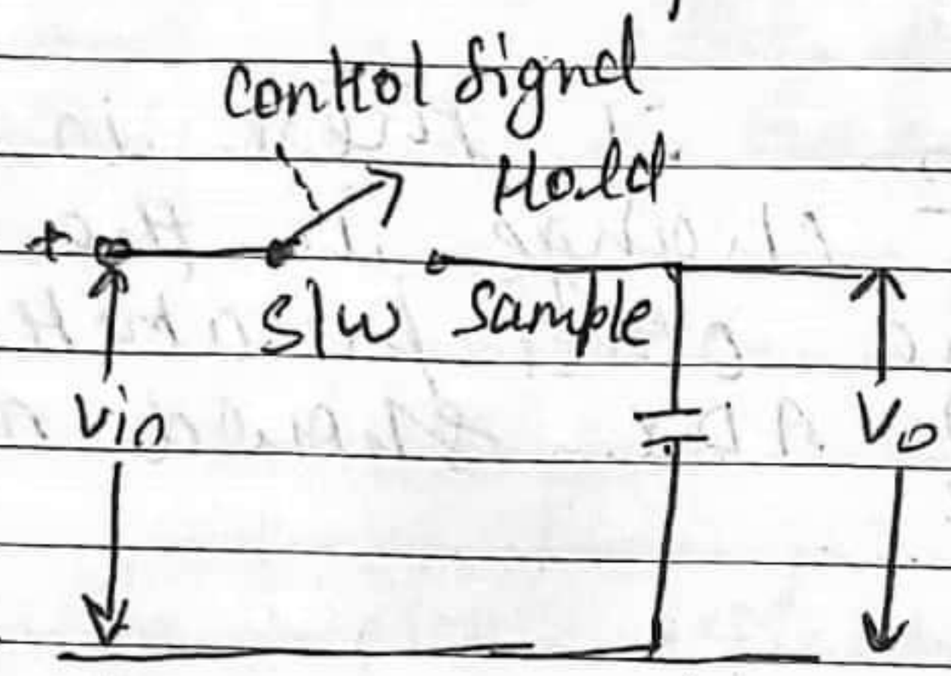
Basic Sample & Hold ckt



Consist of
1. i/p
2. o/p
3. switch
4. capacitor

- Sw controlled by control signal → sw can be BJT or MOSFET → sw is controlled by control voltage → open sw → close sw →

→ Sampling mode → the switch is closed i/p voltage will appear across the capacitor and capacitor is fully charged with instantaneous value (Vin) → this process is called as sampling process →

→ Holding mode → when sw is open → capacitor is now disconnected from input voltage Vin → capacitor has no path to get discharged → so capacitor will hold the value Vin for a certain time period until the switch is closed again.

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Sample & Hold circuit implimentation by using an OPAMP.

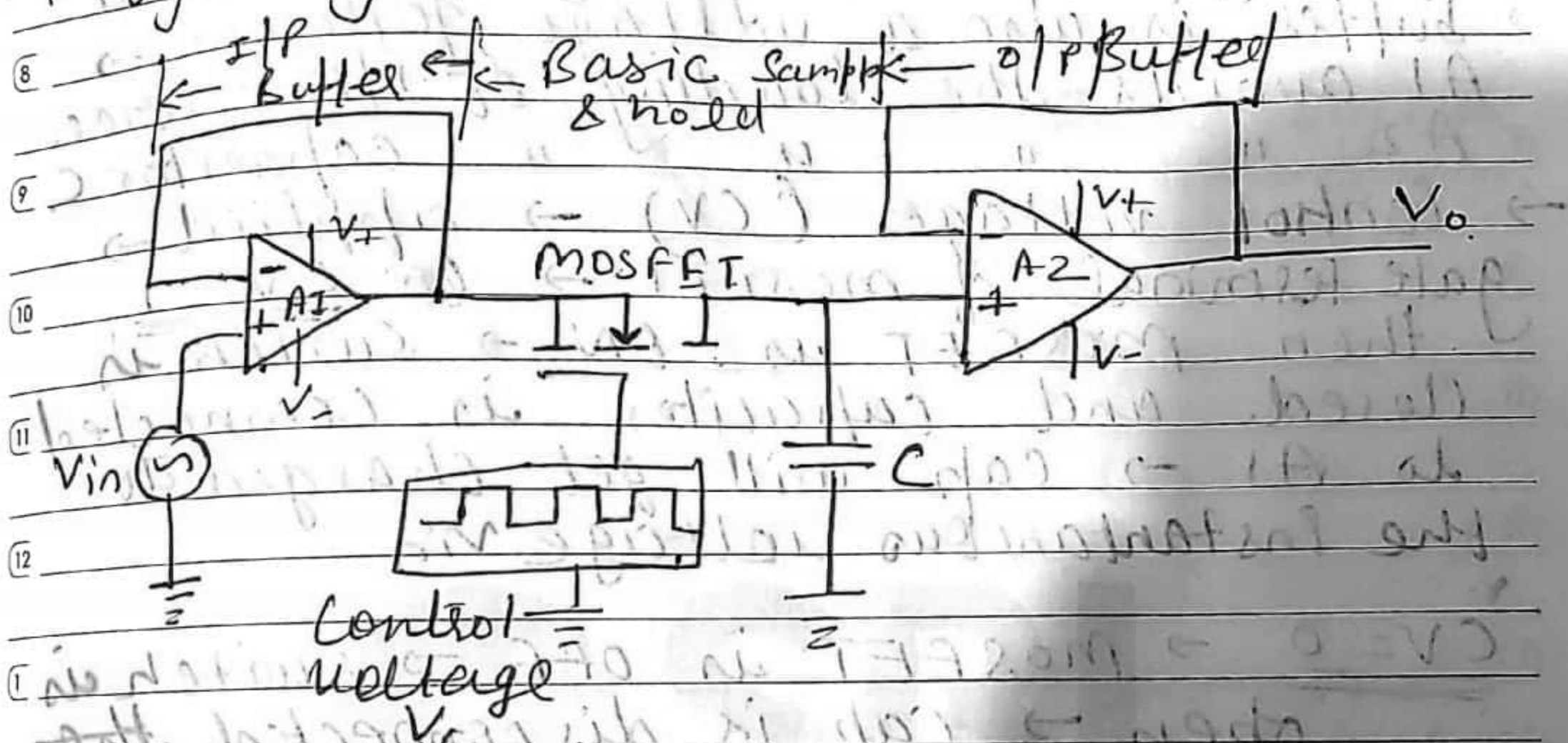

Diagram is divided into 3 Parts.

1. I/P Buffer
2. Basic sample & hold ckt
3. O/P Buffer

Basic Sample & Hold Ckt Consist of MosFET, control signal and a capacitor. Control voltage is applied to the gate terminal of MosFET → so it controls the closing & opening of MosFET and hence switch. So accordingly the capacitor is charged & discharged.

Control voltage = CV.
Switch = SW

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140-225 (WK - 21)

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Working of circuit:

→ I/p buffer is voltage follower → o/p buffer is also a voltage follower → A1 avoids the loading of i/p source A2 " " " " capacitor C. → Control voltage (CV) → applied → gate terminal of MOSFET → if CV = 1 then MOSFET is ON → switch is closed and capacitor is connected to A1 → cap will get charged to the instantaneous voltage Vin

CV = 0 → MOSFET is off → switch is open → cap is disconnected from the input A1 (Vin) → Capacitor cannot discharged from the output buffer (A2) as 2 OPAMP is having high i/p impedance → Capacitor will hold the charge until the next sampling cycle

Waveform

(T) Total time period = $T_s + T_H$

T_s = Sampling time

T_H = Holding time

T = Time duration for the cap will charge the to with the i/p voltage

2019 it perform the sampling process.

Sinusoidal wave.

TH = Time during ∈ the capacitor will hold the input voltage (charge) present on it.

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142-223 (WK - 21)

M T W T F S S
1 2 3 4 5 6 7
8 9 10 11 12 13 14
15 16 17 18 19 20 21
22 23 24 25 26 27 28
29 30

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The capacitor is required to hold the charge so it should be a leak proof capacitor (Teflon and Polyester cap are generally used)

Application

1. In the Pulse modulation
2. In digital Interfacing
3. In ADC
4. In analog Demux.

Quantization and Encoding.

In DAC → no. of i/p are fixed for eg. in 3bit D/A Converter, there are 8 possible inputs.

But in A/D convertor, the i/p analog voltage have any value in a range, but the digital o/p will have 2^N values for N bit A/D convertor.

There for a whole range of analog voltage is required to be present suitable in 2^N intervals. This process is known as Quantization.

Each interval is then assigned a unique N bit binary code → referred to as encoding.

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Example. voltage range - 0 to 1 volt
digital o/p is 3-bit → means
8 possible output values. (0-1 volt)
- so divide the whole range (0-1 volt)
into 8 intervals. called Quantization
- each interval is of 1/8 size. 1/8 size
as shown in fig.

Analog voltag	Equivalent digital value.
8/8 V	
7/8 V	111
6/8 V	110
5/8 V	101
4/8 V	100
3/8 V	011
2/8 V	010
1/8 V	001
0	000

Quantization — Encoding.

- Now the N intervals are represented by unique digital values
- There is an error referred to as quantization error (QE) involved in this process
- QE can be reduced if
middle six intervals size is 1/8 = 5
and top bottom intervals size is = 1/8 / 2

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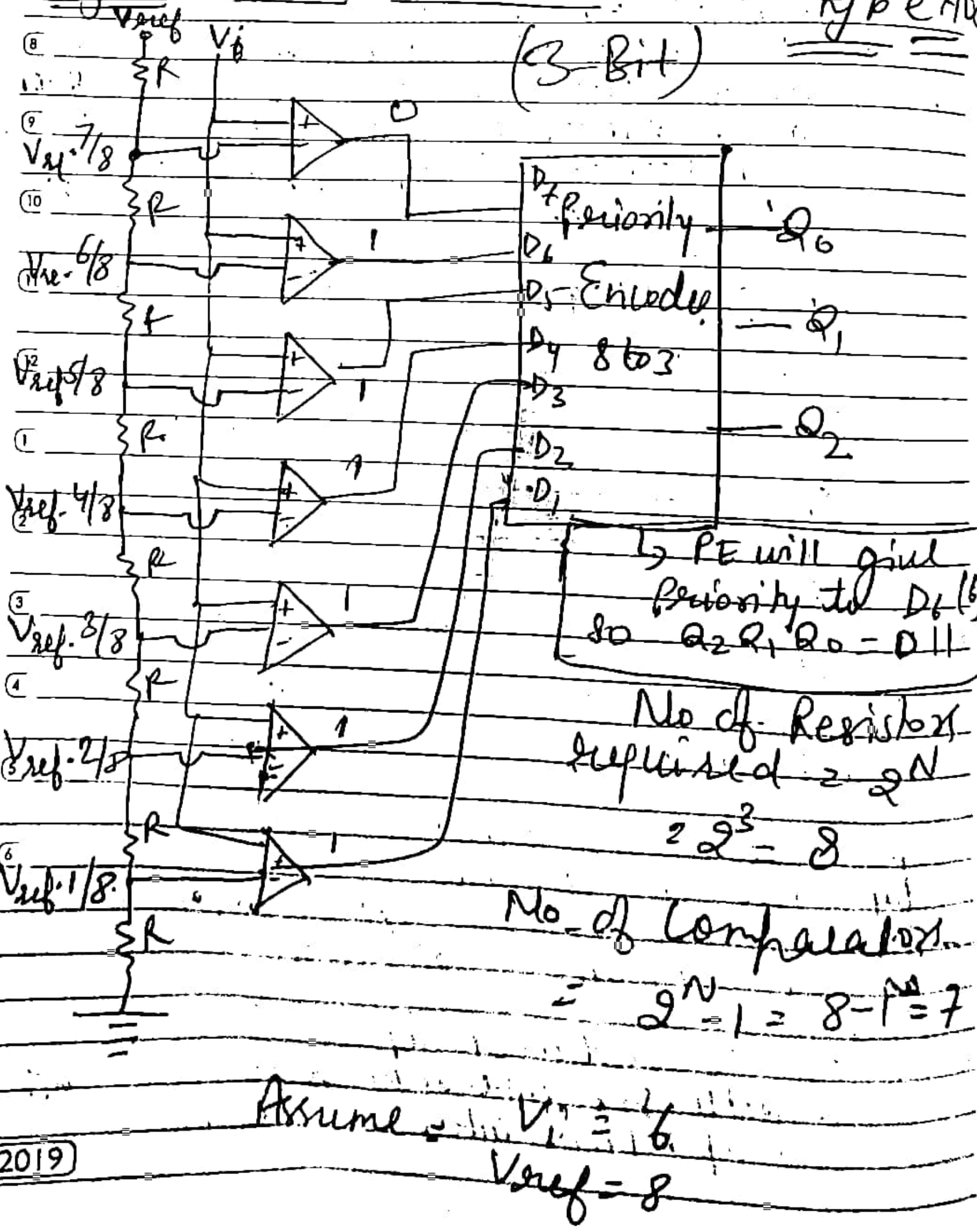
144-221 (WK - 21)

Types of ADC Converter (1) Parallel type ADC (3-Bit)



No of Resistor required = 2^N

$= 2^3 = 8$

No of Comparator

$= 2^N - 1 = 8 - 1 = 7$

Assume $V_i = 6$

$V_{ref} = 8$

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Input to 1st Comparator

(V_{nI}) at non inverting terminal = 6 volt (V_i)

$V(I)$ " inverting " = $V_{ref} \cdot \frac{7}{8}$ =

if $V_{nI} > V_i$ = high o/p = $\frac{8}{8} \times 7 = 7$ volt

if $V_{nI} < V_i$ = low o/p

$V_{nI} = 6$

$V_I = 7$ volt So. o/p of Comp = 0

Input to 2nd comparator -

$V_{nI} = 6$ volt So $V_{nI} = V_I$

$V_I = 6$ volt

So o/p is high.

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147-218 (WK - 22)

M T W T F S S
1 2 3 4 5 6 7
8 9 10 11 12 13 14
15 16 17 18 19 20 21
22 23 24 25 26 27 28
29 30

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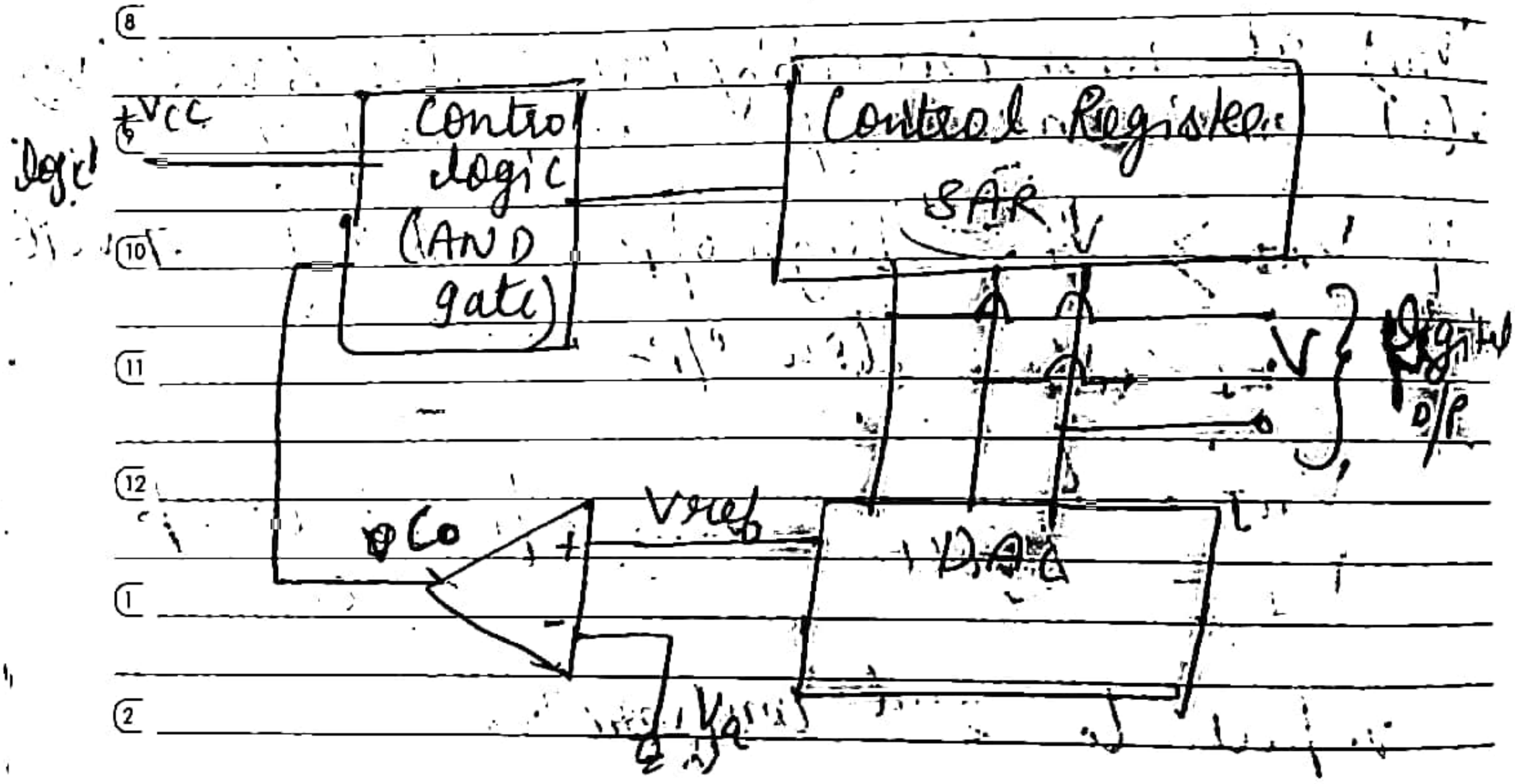
Successive Approximation Type ADC



SAR - Successive approximation register

Control logic provides clock to SAR → That helps it to set & reset

Eg: At the initial stage the o/p of SAR - 000

→ DAC will give Analog voltage of 0V.

Vref = 0 so Va > Vref.

Vo SO Co = 1

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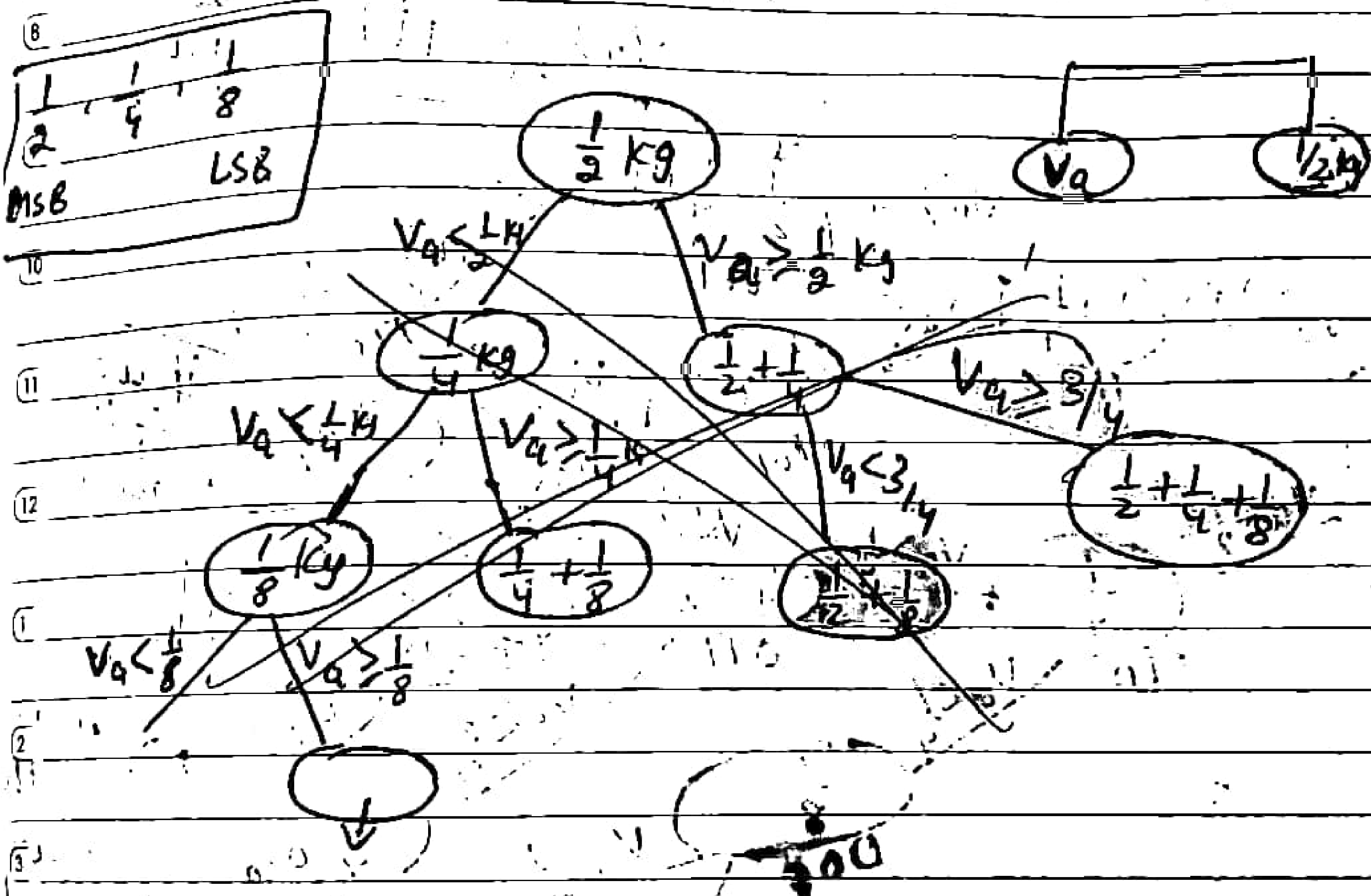
For Comparator:

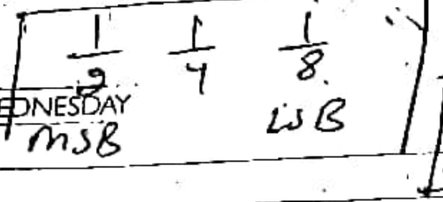
$V_a > V_{ref}$ = O/P is high

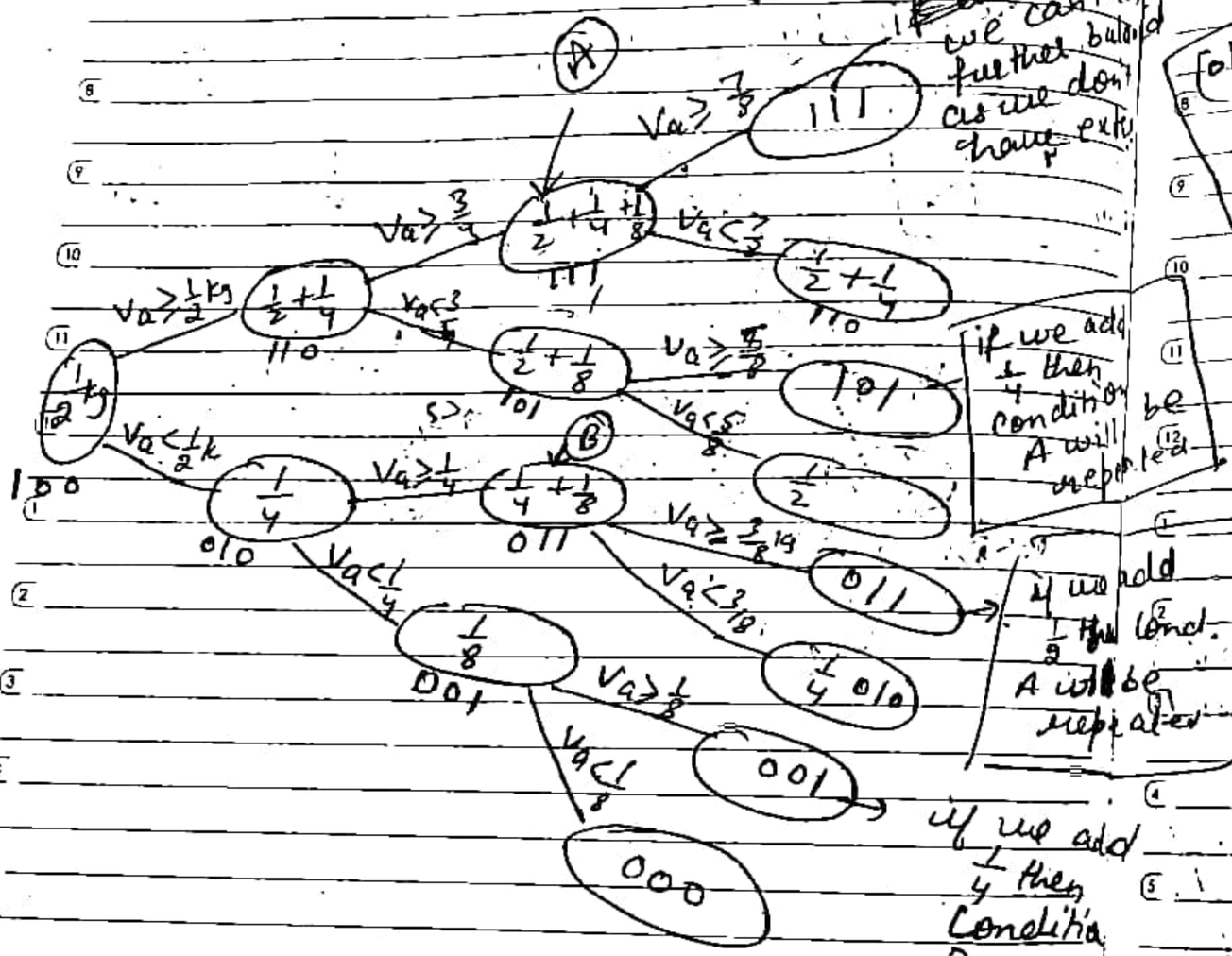
$V_a < V_{ref}$ = O/P is low

V_a = unknown V_{ref} = diff value

V_a = V_a only ; V_{ref} = $\frac{1}{2}$ kg, $\frac{1}{4}$ kg, $\frac{1}{8}$ kg.

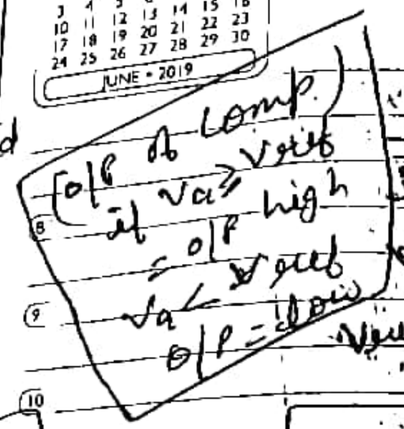




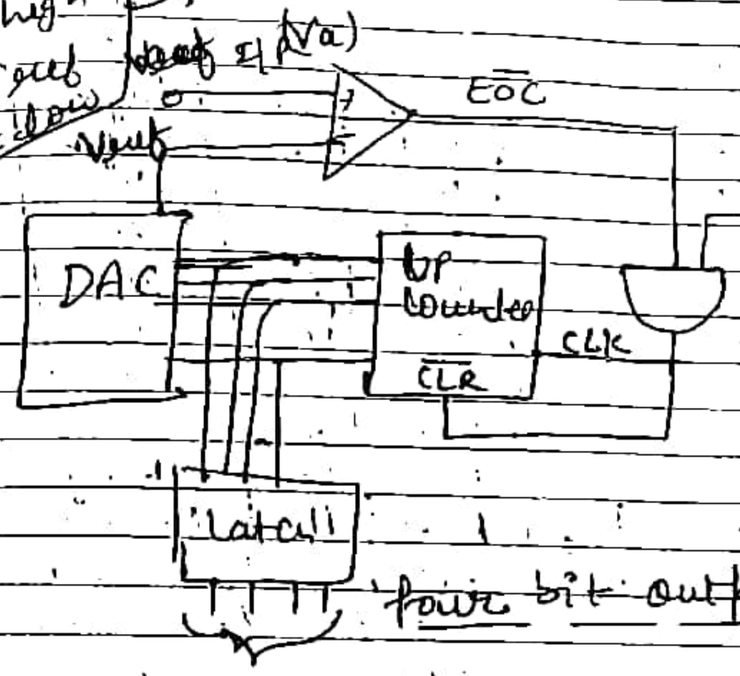


if we add 1/4 then condition A will be repeated

if we add 1/4 then condition B will be repeated



Counter Type ADC



Let's take V_a = 10V
Initial value of Vref = 0.
o/p of comparator = $V_a > V_{ref}$ = high.
1 logic will go to AND gate
o/p of AND gate = 1
Counter will shift its value

0000
↓
0001

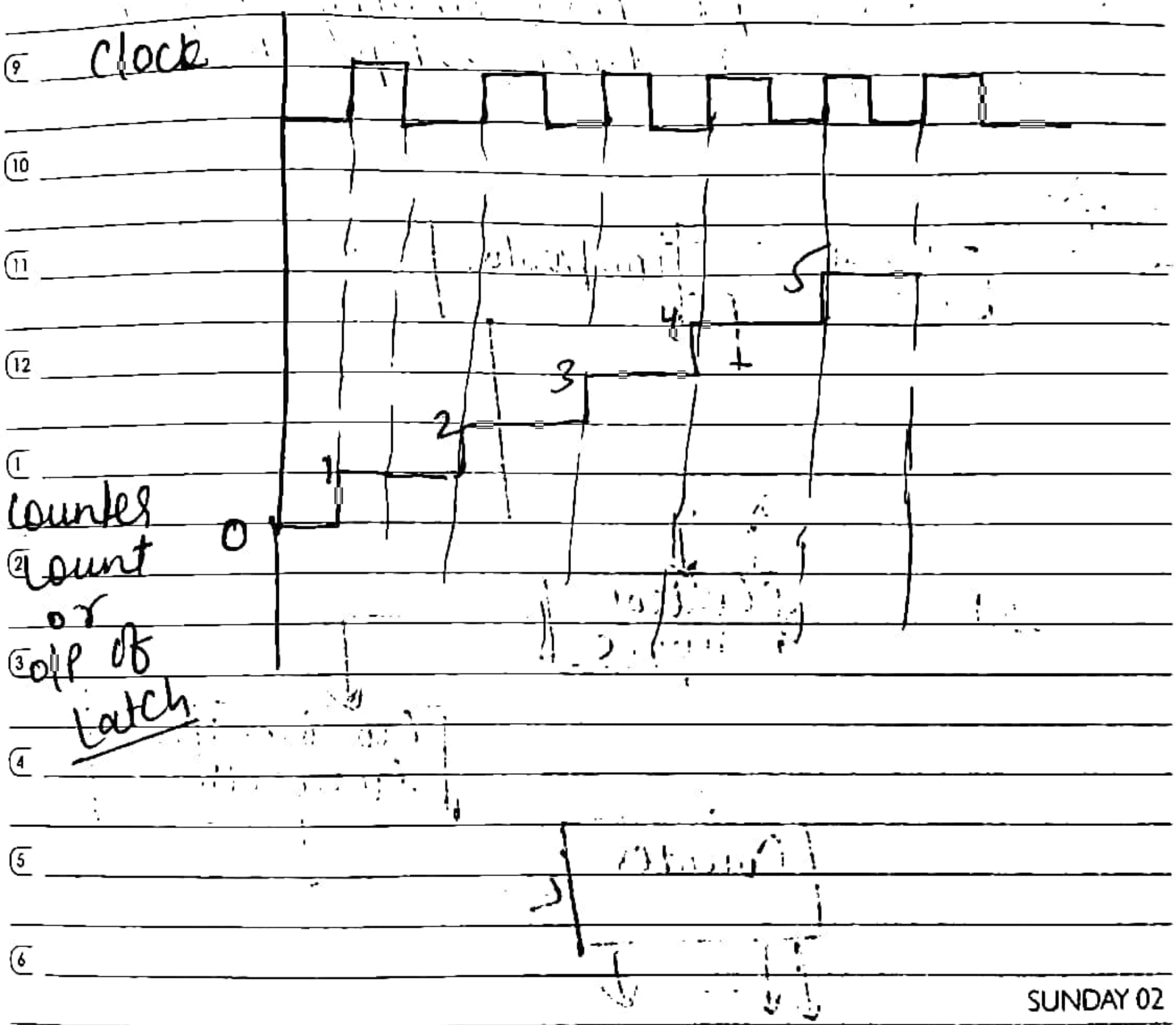
Clock	Counter o/p	Latch value	Vref	When Va=10V Opam o/p
0	0	0000	0	high
1	1	0001	1	high
1	2	0010	2	high
1	3	0011	3	high
1	4	0100	4	"
1	5	0101	5	"
1	6	0110	6	"
1	7	0111	7	"
1	8	1000	8	"
1	9	1001	9	"
1	10	1010	10	"
0	0000	1010	11	low

at this state the o/p of latch will sit to 1010 (low) and the counter will reset to zero value.

Drawback: As incr. ↑ the value of Vref, the time to convert this value into digital value will goes on incr.

In all conversion time is large in case we take Vref as large value.

waveform



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JUNE • MONDAY

154-211 (WK - 23)

M	T	W	T	F	S
		1	2	3	4
6	7	8	9	10	11
13	14	15	16	17	18
20	21	22	23	24	25
27	28	29	30	31	

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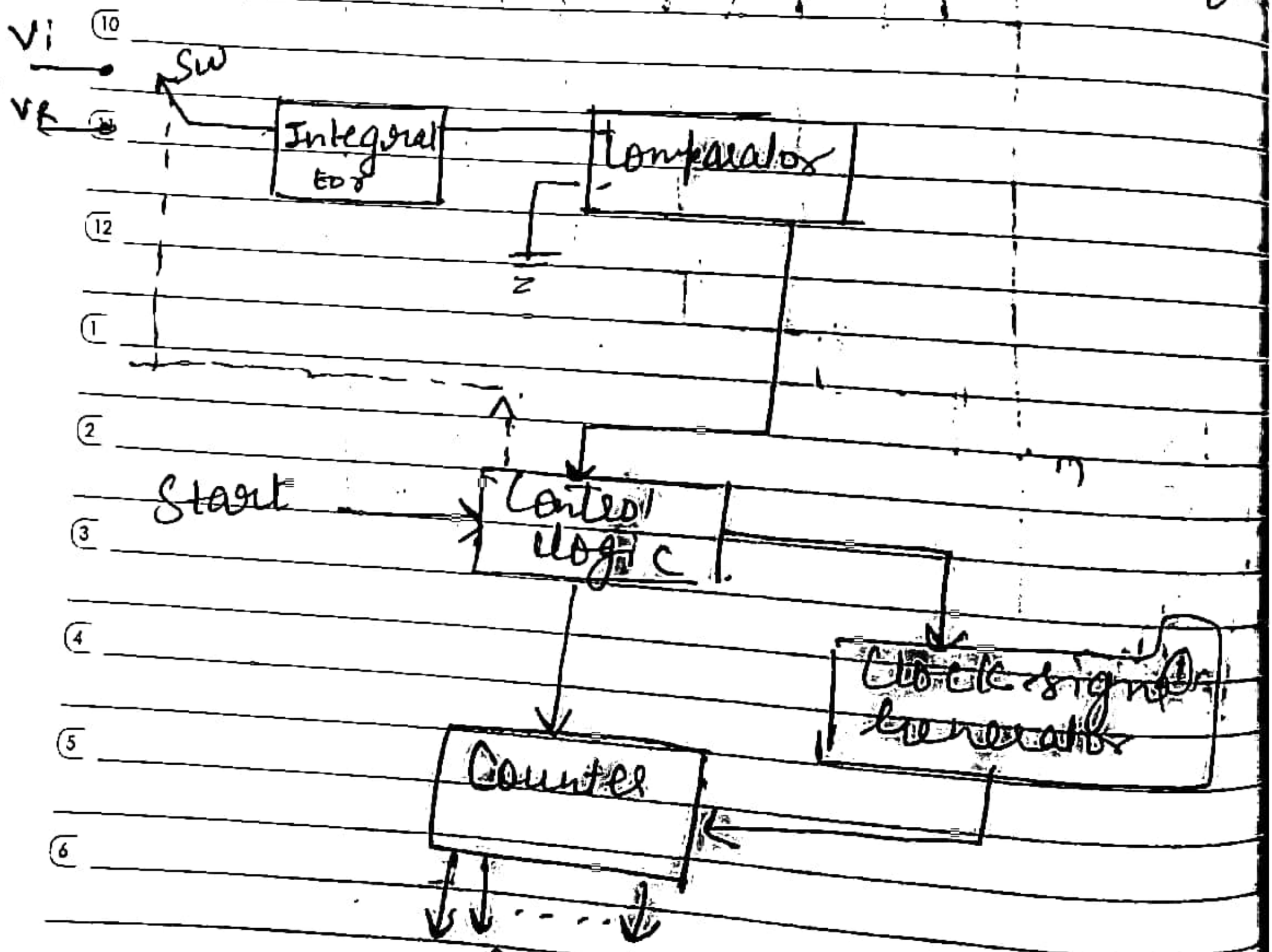
Dual slope ADC

it produces an equivalent digital o/p for a corresponding analog input by using two (dual) slope technique



explaination from tutorial Point website

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